FIG. 1

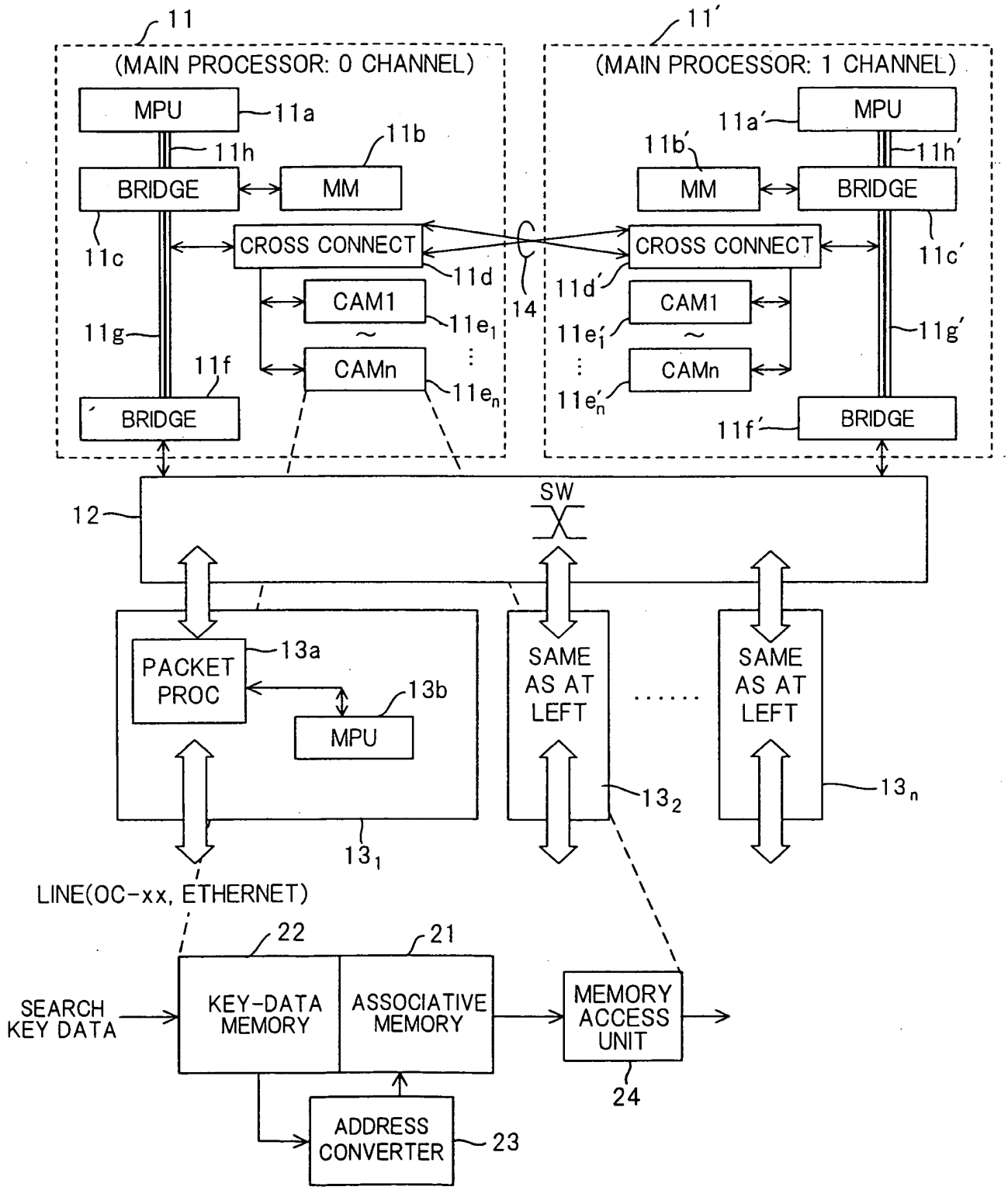
11
(MAIN PROCESSOR: 0 CHANNEL)
MPU
11a
11h
11b
BRIDGE
MM
11c
CROSS CONNECT
11d
CAM1
11e1
11g
11f
CAMn
11en
BRIDGE
11'
(MAIN PROCESSOR: 1 CHANNEL)
11a'
MPU
11h'
11b'
MM
BRIDGE
11c'
CROSS CONNECT
11d'
14
CAM1
11e1'
11g'
CAMn
11en'
11f'
BRIDGE
12
SW
PACKET PROC
13a
13b
MPU
SAME AS AT LEFT
SAME AS AT LEFT
131
132
13n
LINE(OC-xx, ETHERNET)
22
21
SEARCH KEY DATA
KEY-DATA MEMORY
ASSOCIATIVE MEMORY
MEMORY ACCESS UNIT
24
ADDRESS CONVERTER
23

FIG. 2A

TRANSMISSION OF OC-12C PPP PACKET

	ITEMS	VALUE		IP DATA FLUCTUATION	TOTAL TRANSFER TIME(μS)
	OC-12C TRANSFER TIME	1.6		1	0.36
	PPP + FIXED PART OF IP HEADER (bytes)	27		2	0.37
	IP DATA FLUCTUATION (bytes)	n		3	0.39
				4	0.40
	TOTAL TRANSFER TIME = (n + PPP + FIXED PART OF IP) * OC-12C TRANSFER			~	~
				10	0.48
				~	~
				64	1.17
				~	~
				128	1.99
				~	~
				1024	13.52
				~	~
				1500	19.64

FIG. 2B

TRANSMISSION OF OC-192C PPP PACKET

	ITEMS	VALUE		IP DATA FLUCTUATION	TOTAL TRANSFER TIME(μS)
	OC-192C TRANSFER TIME(ns)	0.1		1	0.02
	PPP + FIXED PART OF IP HEADER (bytes)	27		2	0.02
	IP DATA FLUCTUATION (bytes)	n		3	0.02
				4	0.02
	TOTAL TRANSFER TIME = (n + PPP + FIXED PART OF IP) * OC-192C TRANSFER			~	~
				10	0.03
				~	~
				64	0.07
				~	~
				128	0.12
				~	~
				1024	0.84
				~	~
				1500	1.23

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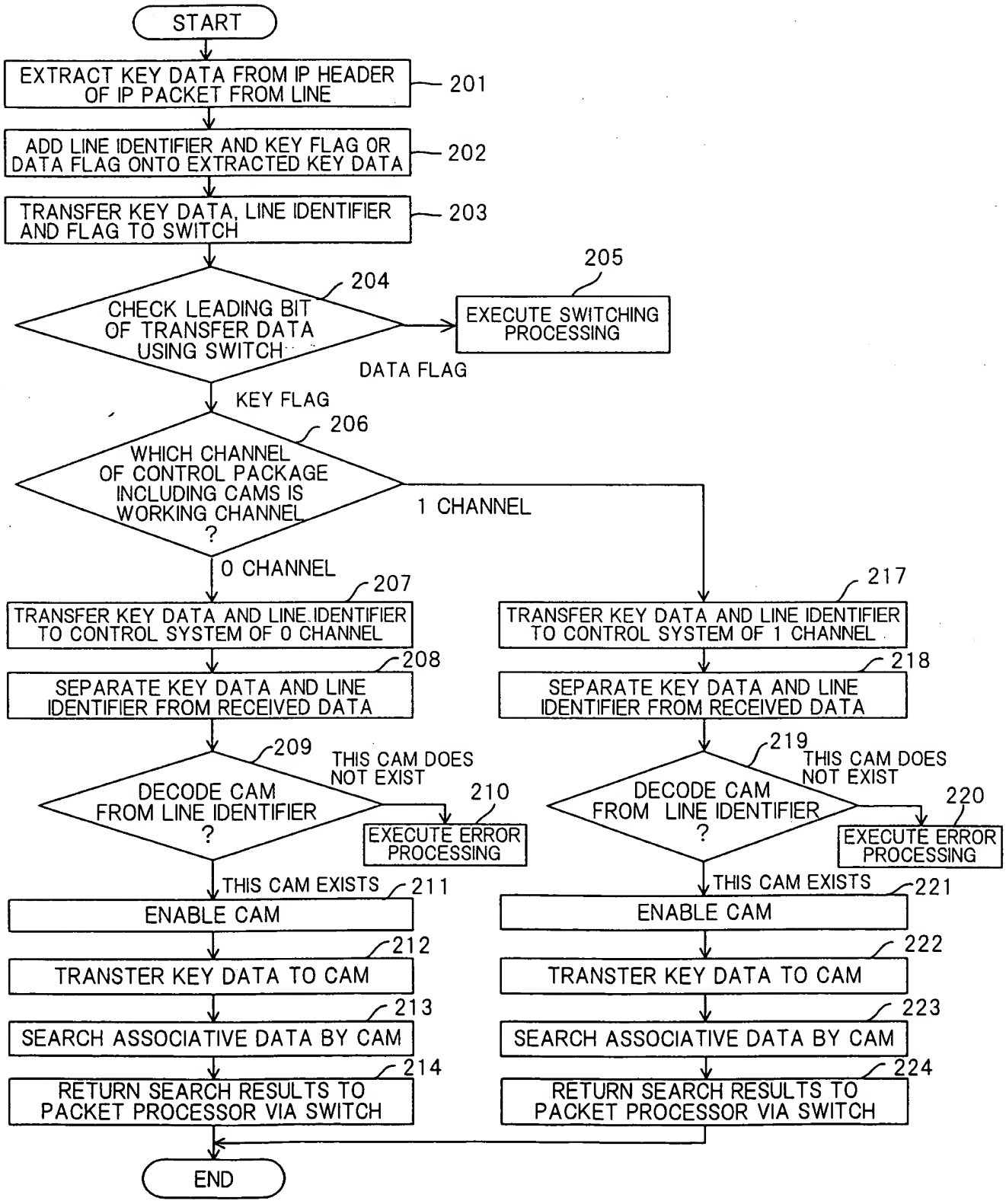
FIG. 3



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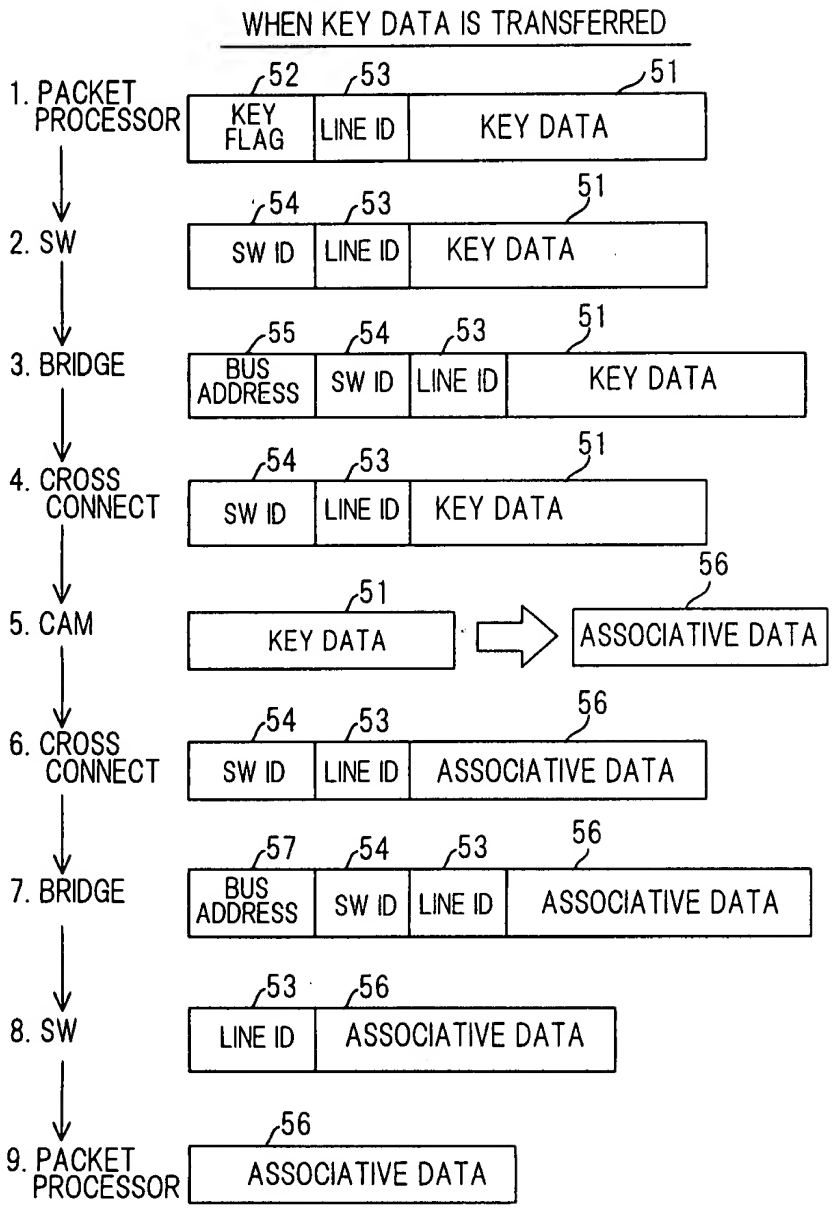
WHEN KEY DATA IS TRANSFERRED
1. PACKET PROCESSOR
KEY FLAG
LINE ID
KEY DATA
52
53
51
2. SW
SW ID
LINE ID
KEY DATA
54
53
51
3. BRIDGE
BUS ADDRESS
SW ID
LINE ID
KEY DATA
55
54
53
51
4. CROSS CONNECT
SW ID
LINE ID
KEY DATA
54
53
51
5. CAM
KEY DATA
ASSOCIATIVE DATA
51
56
6. CROSS CONNECT
SW ID
LINE ID
ASSOCIATIVE DATA
54
53
56
7. BRIDGE
BUS ADDRESS
SW ID
LINE ID
ASSOCIATIVE DATA
57
54
53
56
8. SW
LINE ID
ASSOCIATIVE DATA
53
56
9. PACKET PROCESSOR
ASSOCIATIVE DATA
56

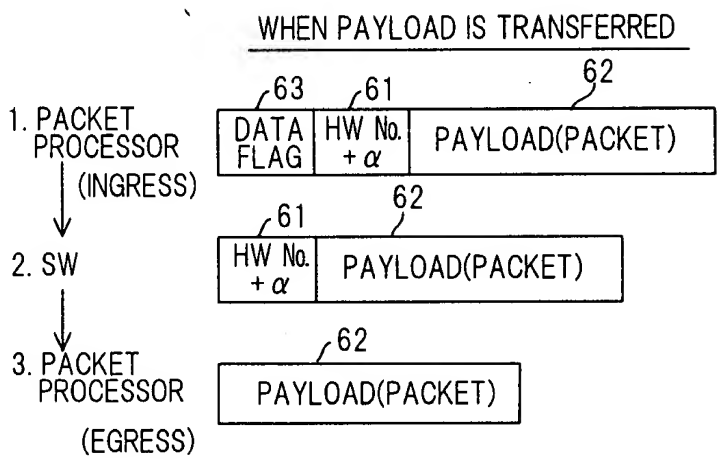
WHEN PAYLOAD IS TRANSFERRED
1. PACKET PROCESSOR (INGRESS)
DATA FLAG
HW No. + α
PAYLOAD(PACKET)
63
61
62
2. SW
HW No. + α
PAYLOAD(PACKET)
61
62
3. PACKET PROCESSOR (EGRESS)
PAYLOAD(PACKET)
62

FIG. 5

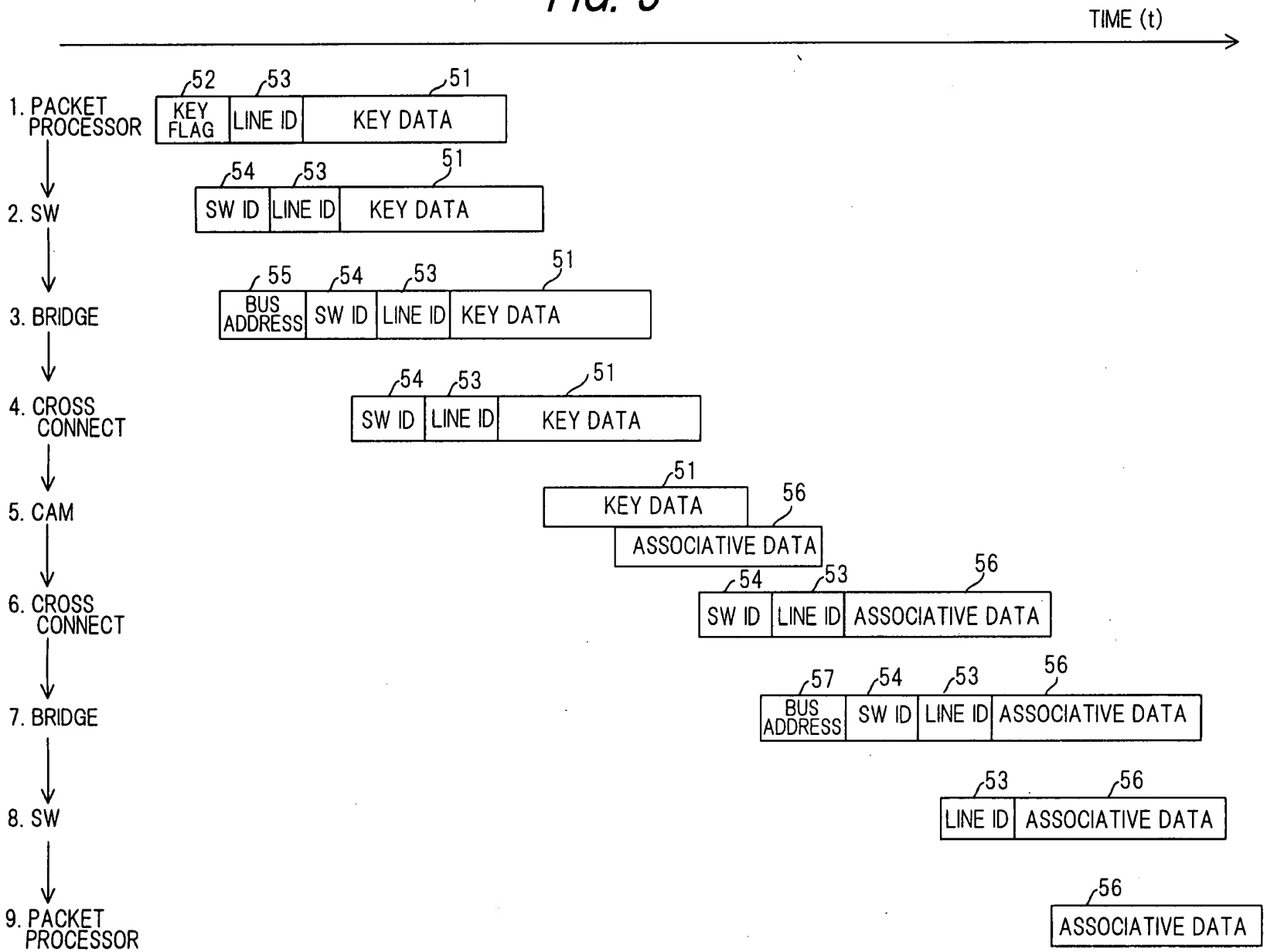
TIME (t)
1. PACKET PROCESSOR
2. SW
3. BRIDGE
4. CROSS CONNECT
5. CAM
6. CROSS CONNECT
7. BRIDGE
8. SW
9. PACKET PROCESSOR
KEY FLAG
LINE ID
KEY DATA
SW ID
BUS ADDRESS
ASSOCIATIVE DATA
52
53
51
54
55
56
57

FIG. 6

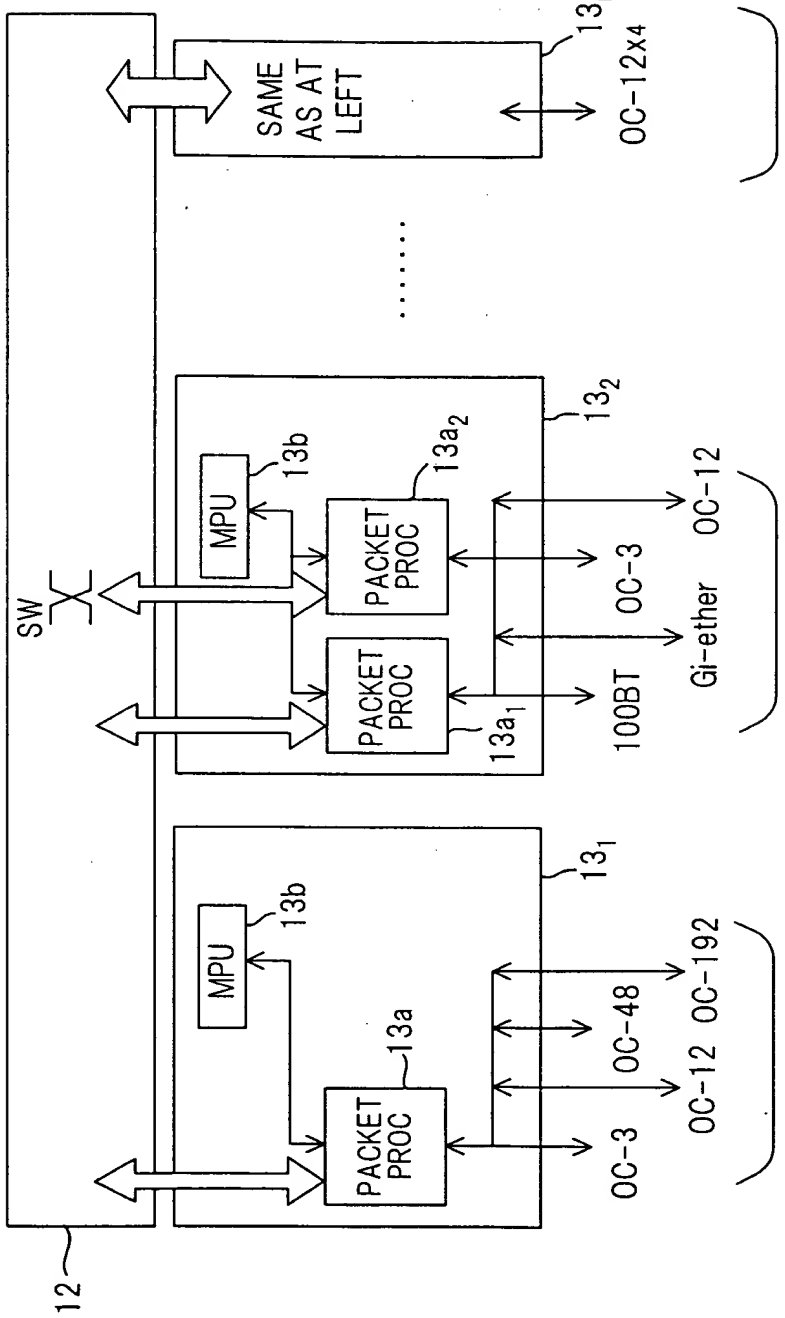
12
SW
MPU
13b
PACKET PROC
13a
13_1
OC-3
OC-12
OC-48
OC-192
$13a_1$
$13a_2$
13_2
100BT
OC-3
Gi-ether
OC-12
SAME AS AT LEFT
13_n
OC-12x4

FIG. 7

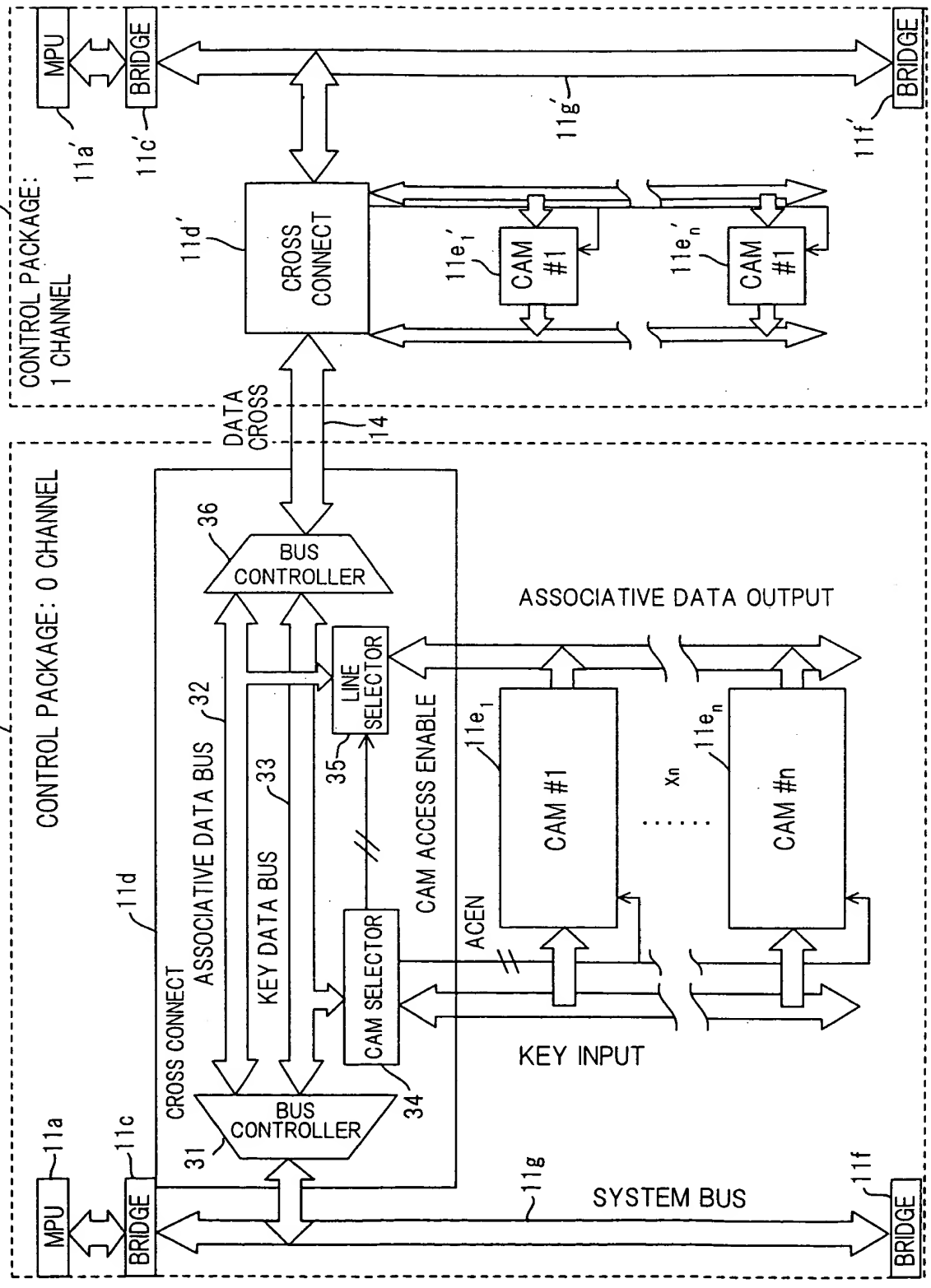
11'
CONTROL PACKAGE:
1 CHANNEL
MPU
11a'
BRIDGE
11c'
11g'
BRIDGE
11f'
11d'
CROSS
CONNECT
11e1'
CAM
#1
11en'
CAM
#1
DATA
CROSS
14
11
CONTROL PACKAGE: 0 CHANNEL
36
BUS
CONTROLLER
ASSOCIATIVE DATA OUTPUT
LINE
SELECTOR
32
35
33
11e1
CAM #1
xn
11en
CAM #n
11d
CROSS CONNECT
ASSOCIATIVE DATA BUS
KEY DATA BUS
CAM ACCESS ENABLE
ACEN
CAM SELECTOR
34
KEY INPUT
31
BUS
CONTROLLER
11a
MPU
11c
BRIDGE
11g
SYSTEM BUS
11f
BRIDGE

FIG. 8

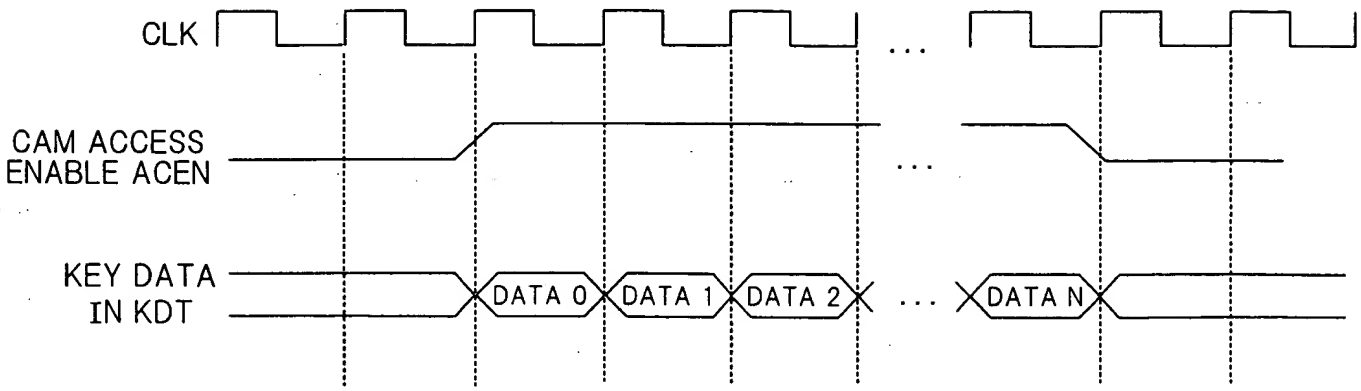

FIG. 11

RAM CELL WIDTH (bytes)		1	1
RAM CELL WORD COUNT	y	1,000	16,384
KEY DATA WIDTH (bytes)	k	4	16
ASSOCIATIVE DATA WIDTH (bytes)	r	2	2
TOTAL ENTRY COUNT		↓	↓
e=y/(k+r)	=	167	910

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FIG. 9

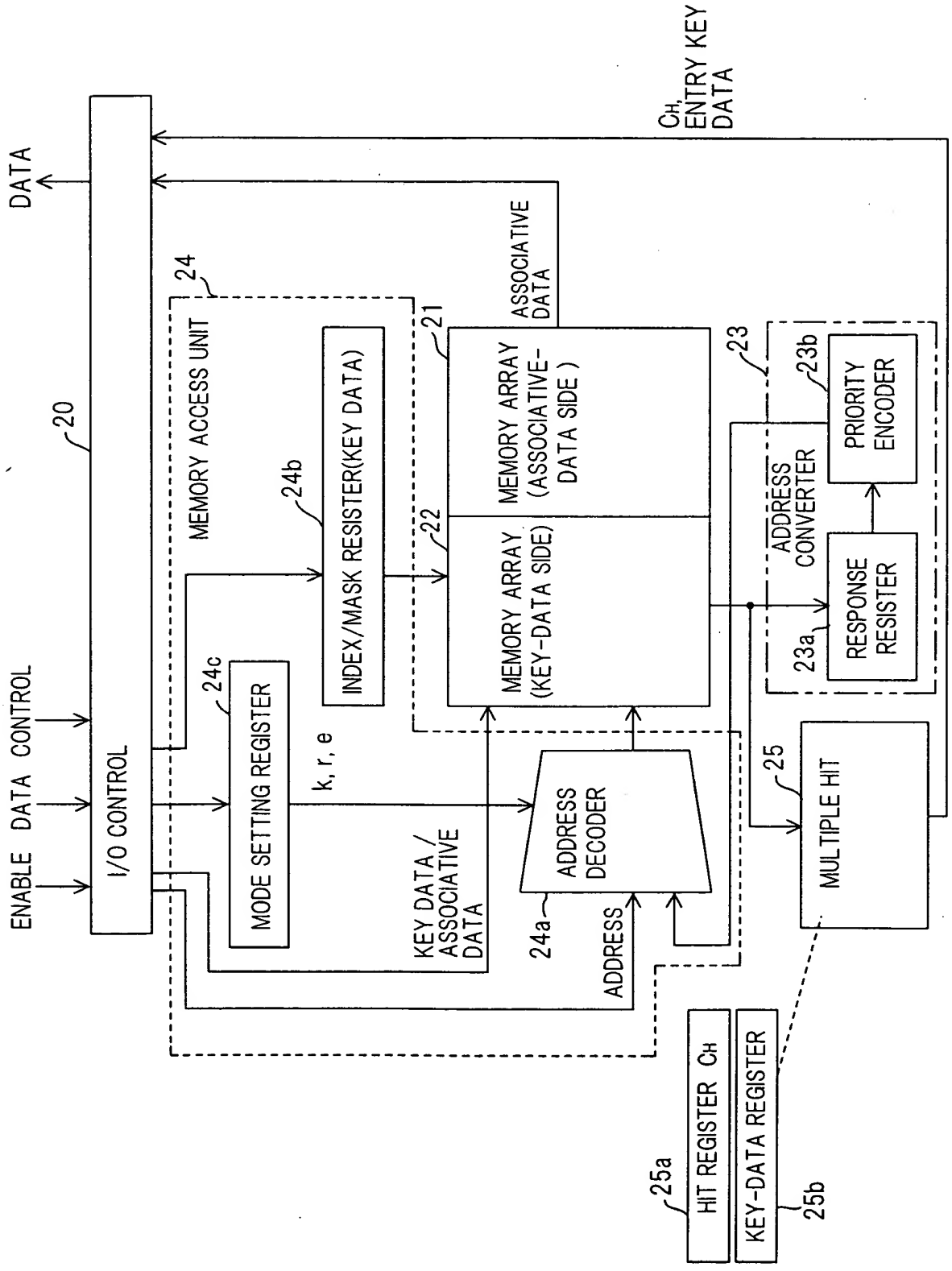

FIG. 10

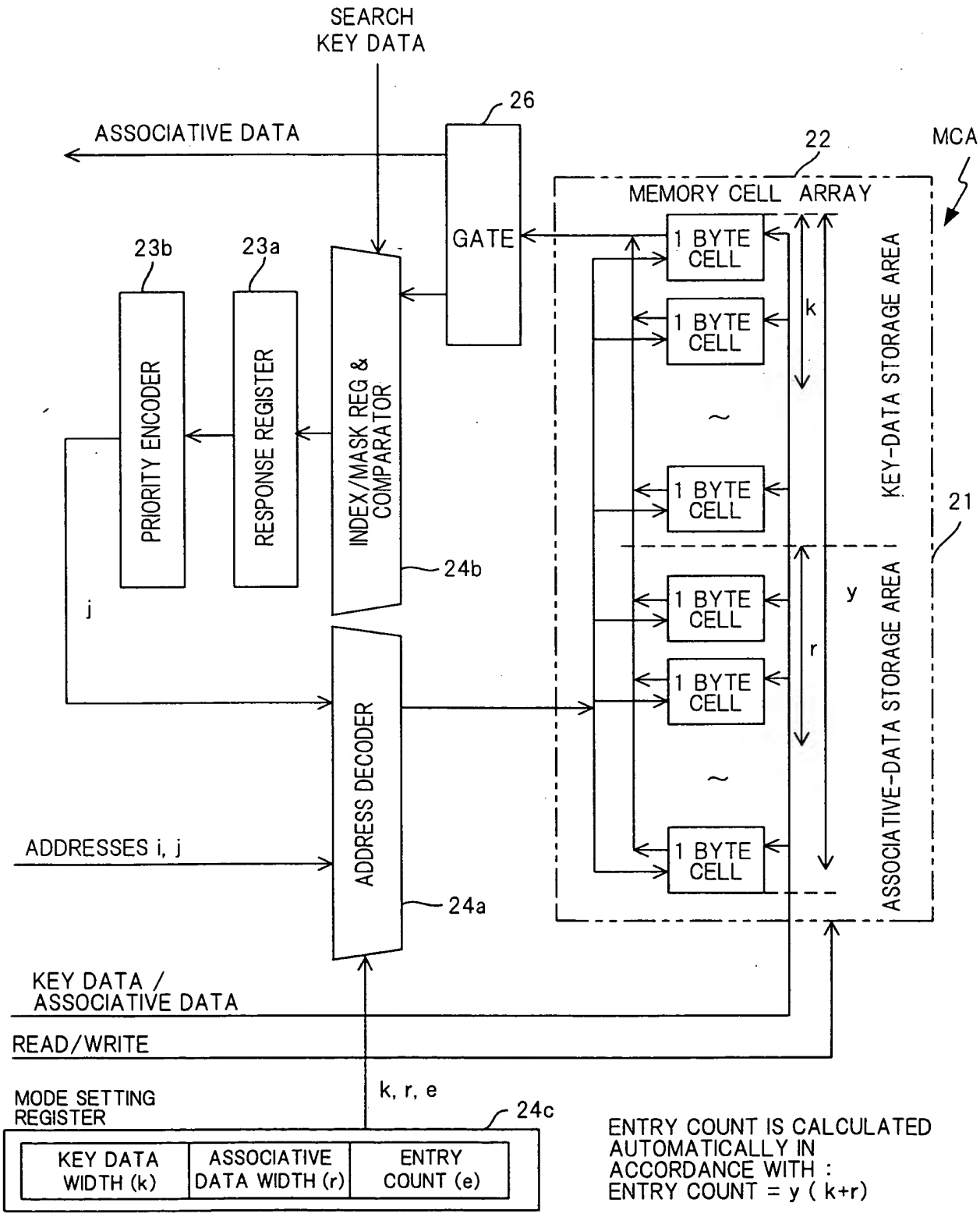
SEARCH KEY DATA
ASSOCIATIVE DATA
26
GATE
22
MCA
MEMORY CELL ARRAY
1 BYTE CELL
k
KEY-DATA STORAGE AREA
21
23b
PRIORITY ENCODER
23a
RESPONSE REGISTER
INDEX/MASK REG & COMPARATOR
24b
j
y
r
ASSOCIATIVE-DATA STORAGE AREA
ADDRESS DECODER
ADDRESSES i, j
24a
KEY DATA / ASSOCIATIVE DATA
READ/WRITE
MODE SETTING REGISTER
k, r, e
24c
KEY DATA WIDTH (k)
ASSOCIATIVE DATA WIDTH (r)
ENTRY COUNT (e)
ENTRY COUNT IS CALCULATED AUTOMATICALLY IN ACCORDANCE WITH :
ENTRY COUNT = y (k+r)

FIG. 12

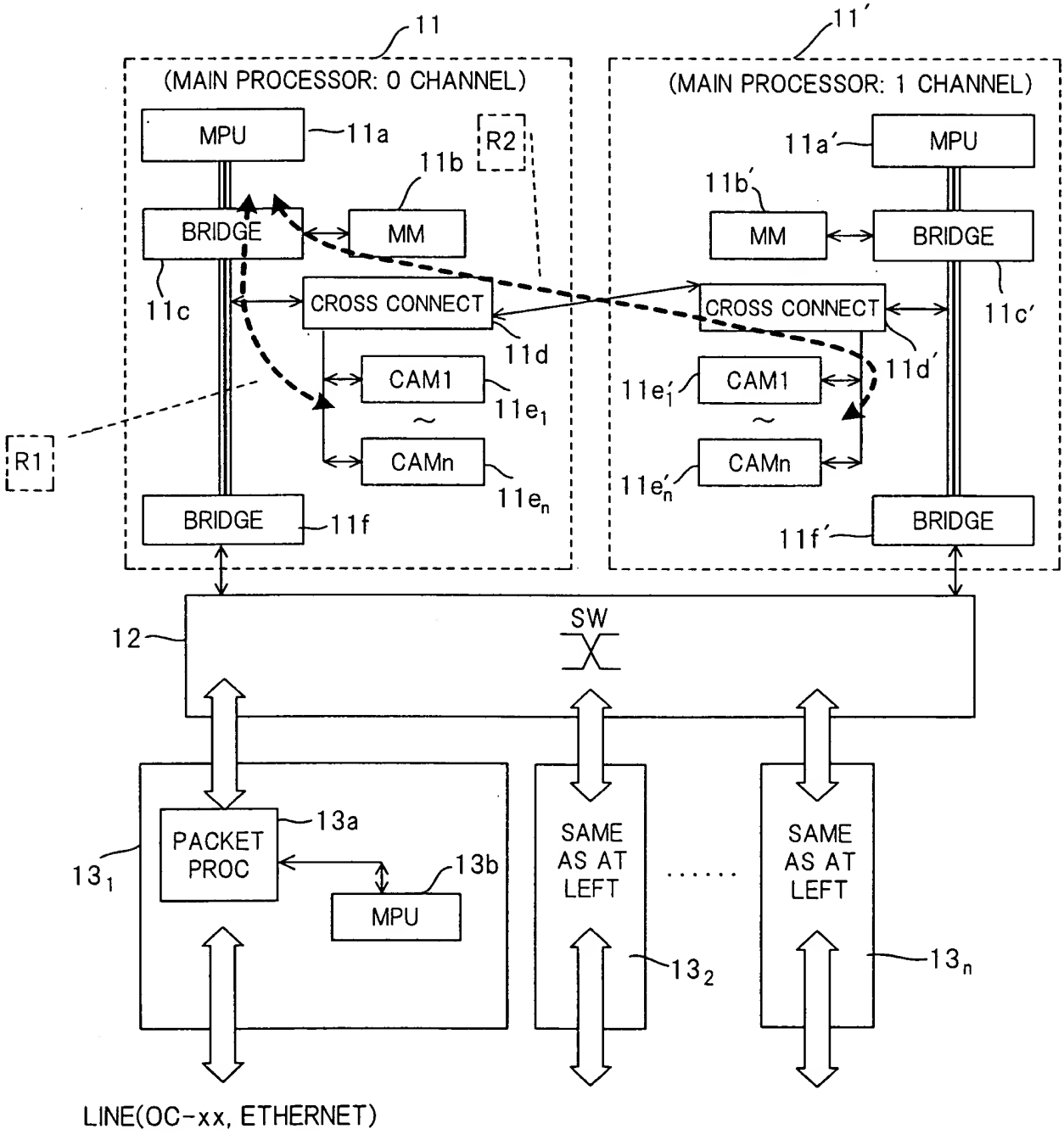
11
(MAIN PROCESSOR: 0 CHANNEL)
MPU
11a
R2
11b
BRIDGE
MM
11c
CROSS CONNECT
11d
CAM1
11e1
CAMn
11en
R1
BRIDGE
11f
11'
(MAIN PROCESSOR: 1 CHANNEL)
11a'
MPU
11b'
MM
BRIDGE
11c'
CROSS CONNECT
11d'
11e1'
CAM1
11en'
CAMn
11f'
BRIDGE
12
SW
PACKET PROC
13a
13b
MPU
131
SAME AS AT LEFT
132
SAME AS AT LEFT
13n
LINE(OC-xx, ETHERNET)

FIG. 13

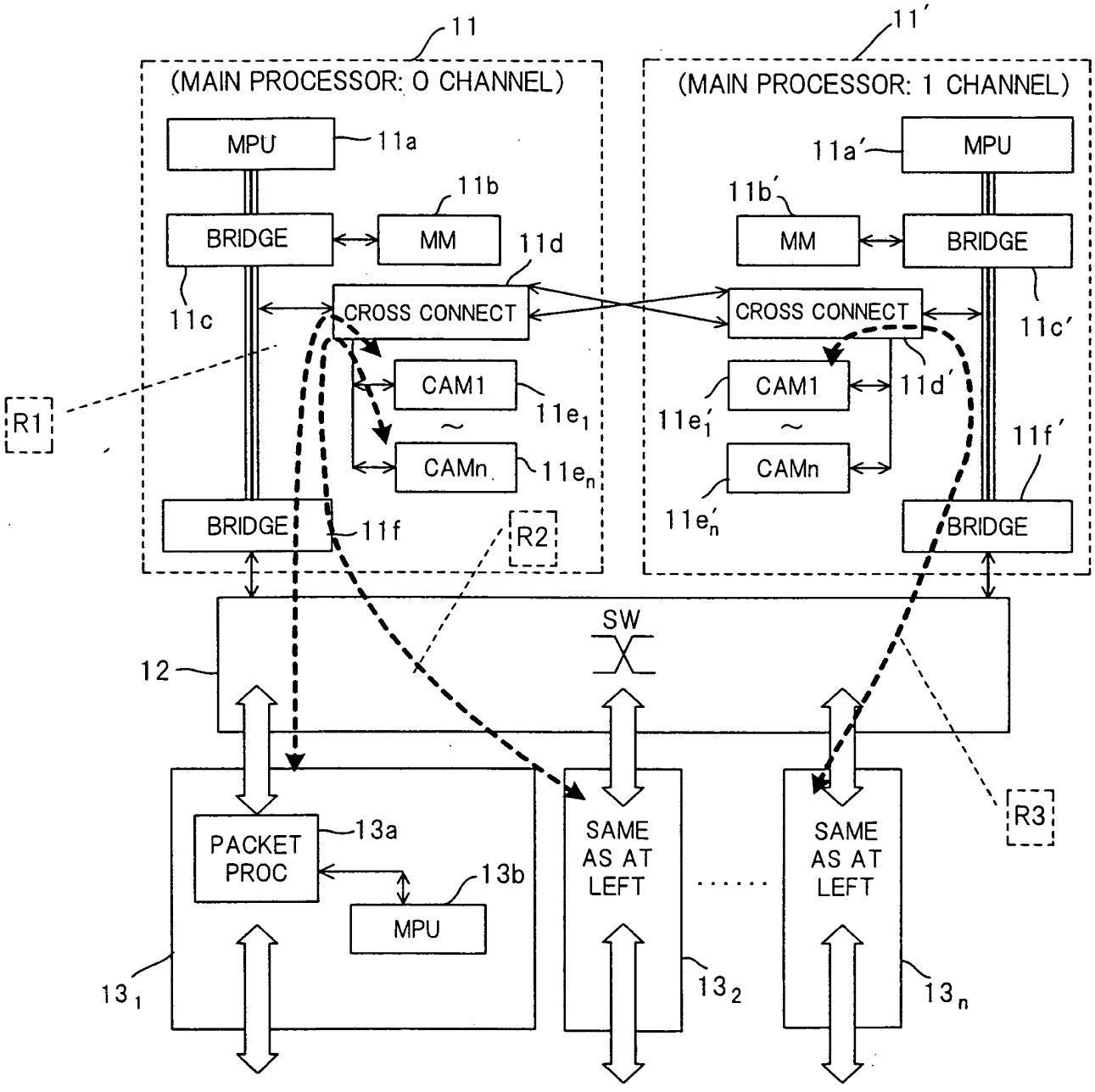
11
(MAIN PROCESSOR: 0 CHANNEL)
MPU
11a
11b
BRIDGE
MM
11d
11c
CROSS CONNECT
CAM1
11e1
CAMn
11en
BRIDGE
11f
R1
R2
11'
(MAIN PROCESSOR: 1 CHANNEL)
11a'
MPU
11b'
MM
BRIDGE
11c'
CROSS CONNECT
CAM1
11d'
11e1'
CAMn
11en'
11f'
BRIDGE
SW
12
PACKET PROC
13a
13b
MPU
SAME AS AT LEFT
SAME AS AT LEFT
R3
131
132
13n
LINE(OC-xx, ETHERNET)

FIG. 14

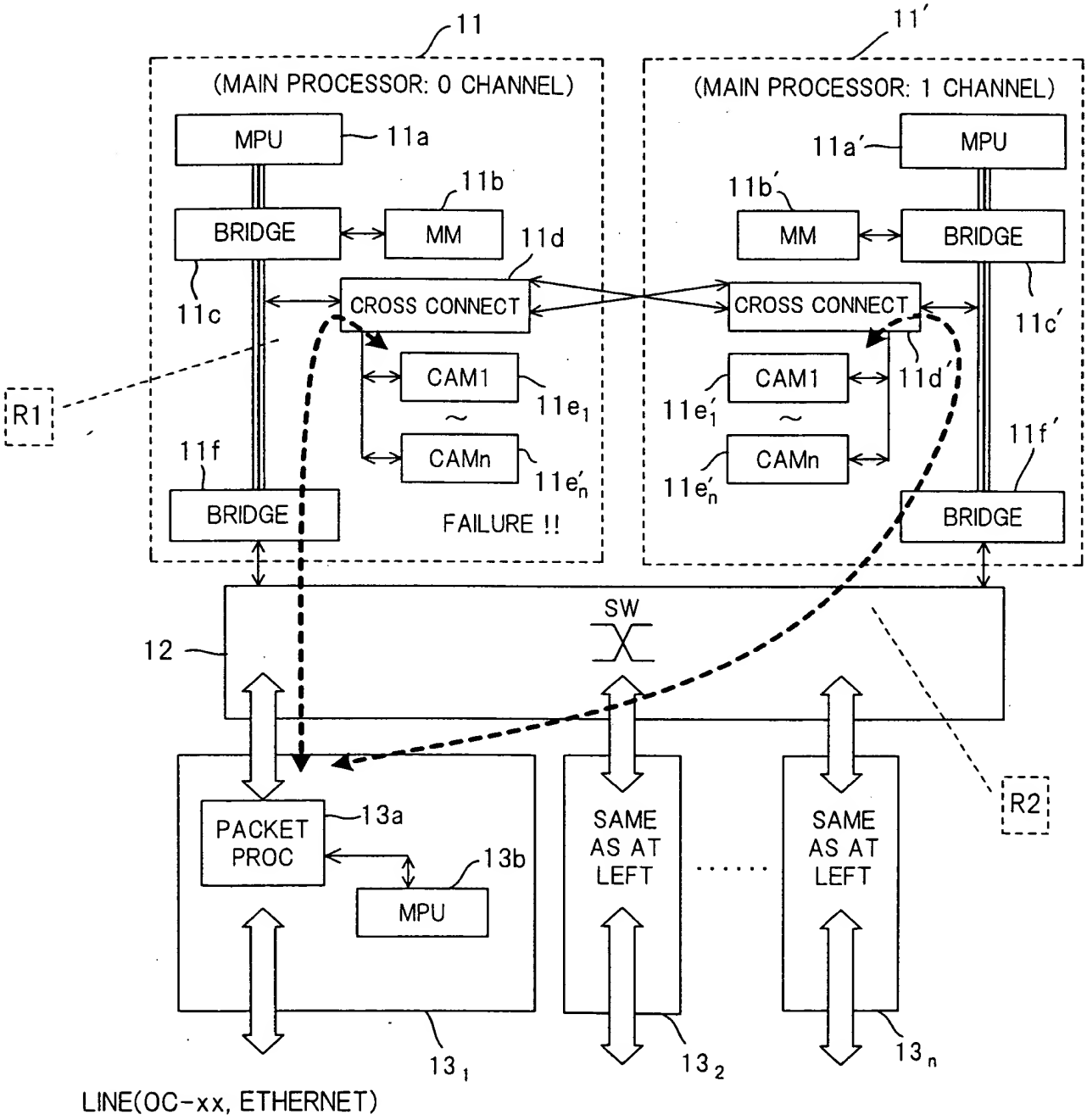
11
(MAIN PROCESSOR: 0 CHANNEL)
MPU
11a
11b
BRIDGE
MM
11d
11c
CROSS CONNECT
CAM1
11e1
CAMn
11e'n
11f
BRIDGE
FAILURE !!
11'
(MAIN PROCESSOR: 1 CHANNEL)
11a'
MPU
11b'
MM
BRIDGE
11c'
CROSS CONNECT
CAM1
11d'
11e'1
CAMn
11e'n
11f'
BRIDGE
R1
12
SW
R2
PACKET PROC
13a
13b
MPU
SAME AS AT LEFT
SAME AS AT LEFT
131
132
13n
LINE(OC-xx, ETHERNET)

FIG. 15 PRIOR ART

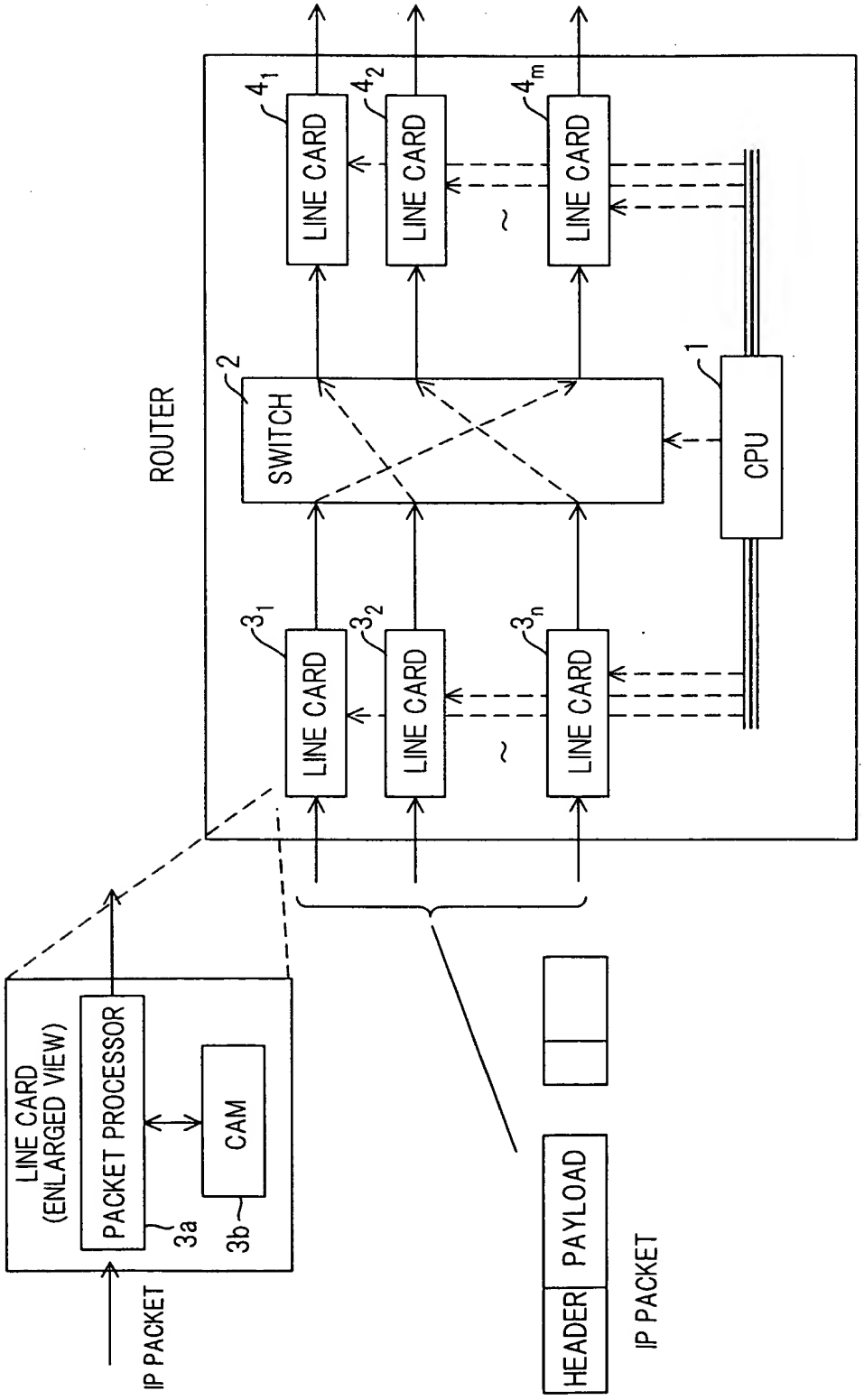

FIG. 16 PRIOR ART

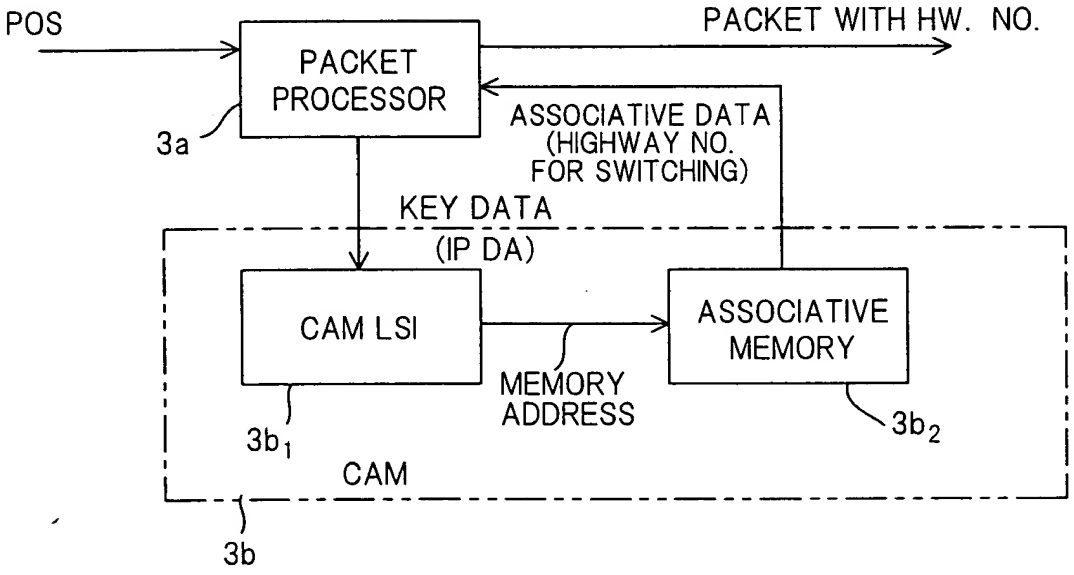

FIG. 17 PRIOR ART

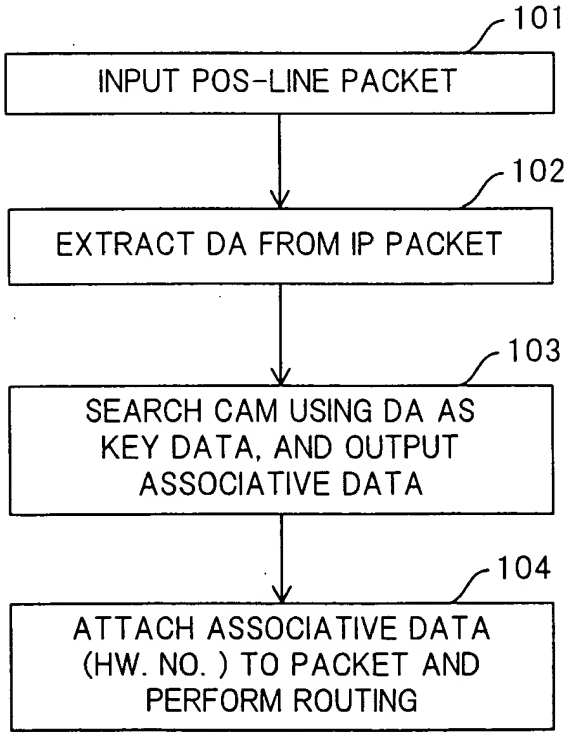

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FIG. 18 PRIOR ART

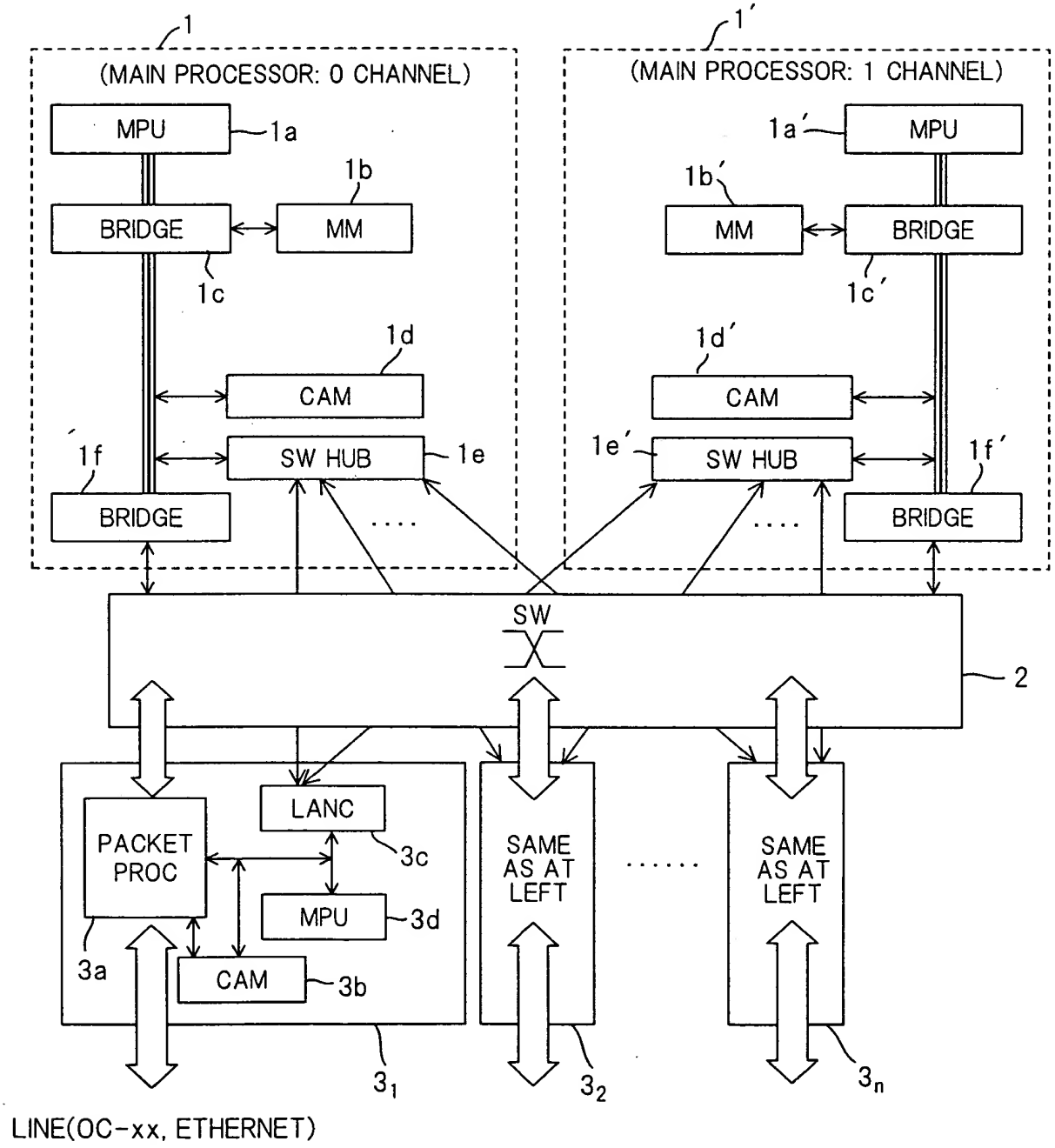
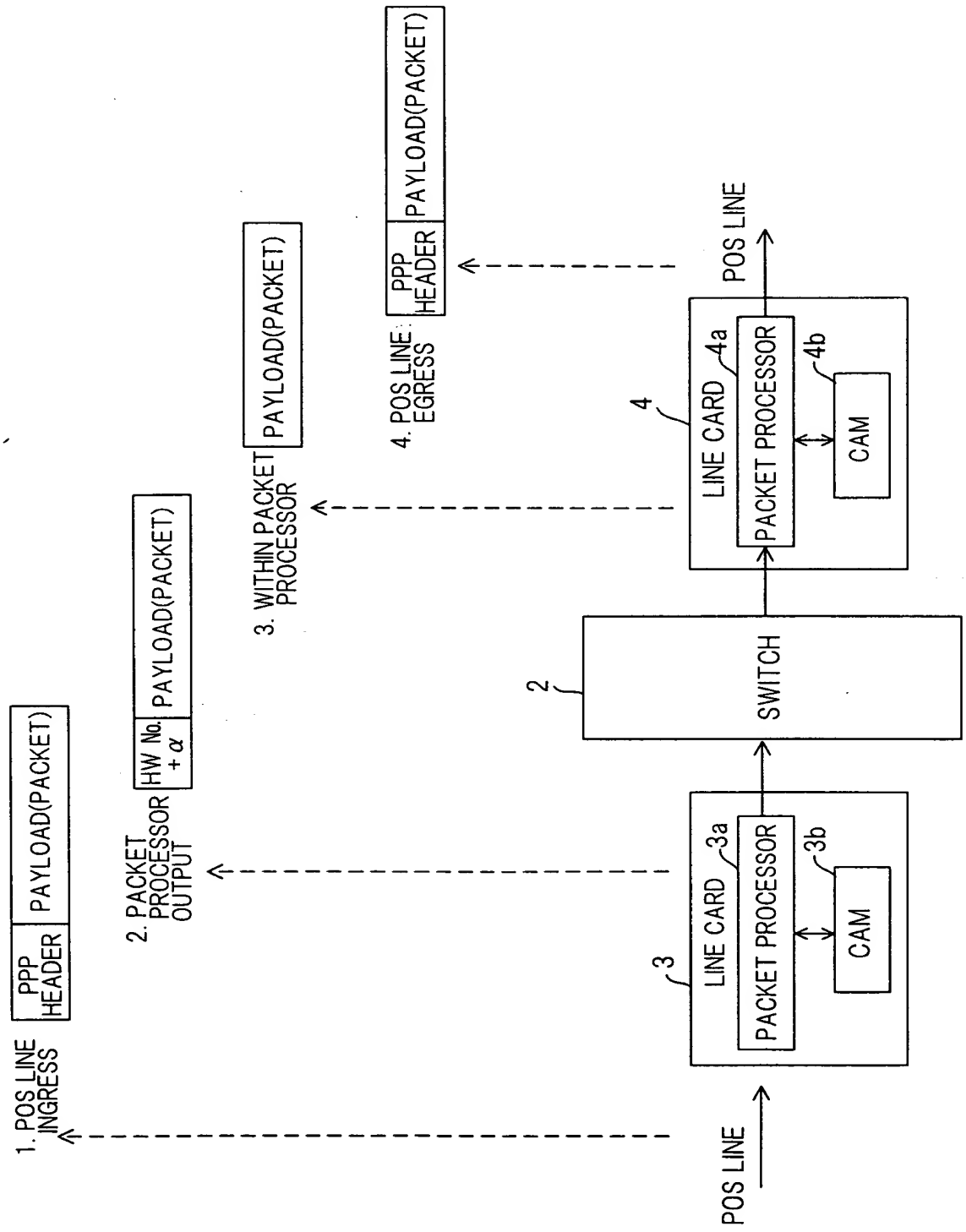


FIG. 19 PRIOR ART



EDGE-20E/9460

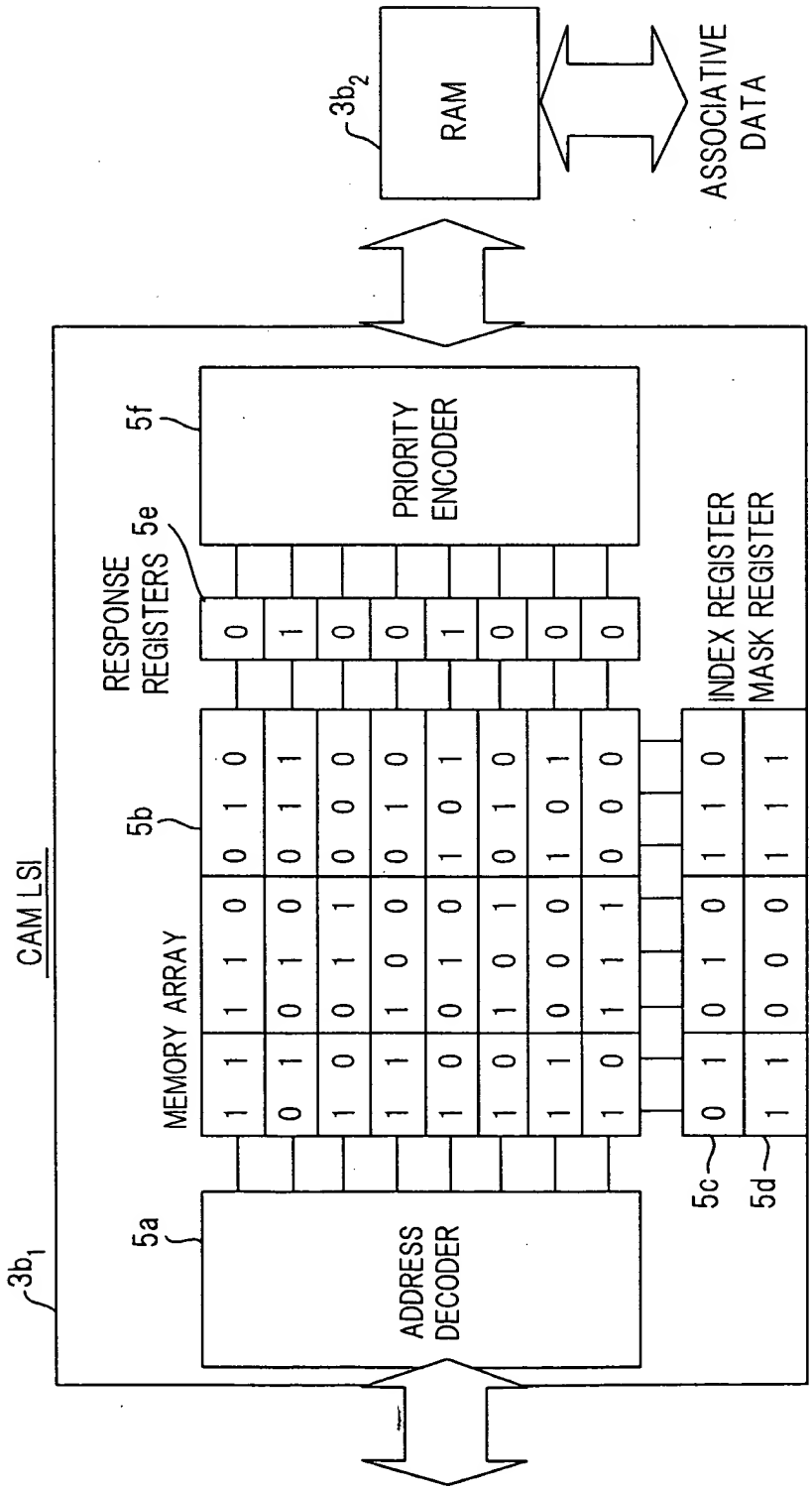



FIG. 20 PRIOR ART